Towards Agile Development of Efficient Deep Learning Operators

Keren Zhou & Philippe Tillet
Transform DNNs to Low Level Code

```
a = torch.randn(64, 32)
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__global__
void mm(float *a, float *b,
float *c) {
    float *a_tile;
    float *b_tile;
    ...
}
```
Transform DNNs to Low Level Code

Model
- PyTorch
- TensorFlow
- JAX

Graph
- XLA/HLO
- TVM/Relay
- PyTorch/fx

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## A Large Number of Tensor Operators

<table>
<thead>
<tr>
<th>Linear</th>
<th>Convolution</th>
<th>Normalization</th>
<th>Embedding</th>
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</thead>
<tbody>
<tr>
<td>◆ Fused</td>
<td>◆ Depthwise</td>
<td>◆ Batch</td>
<td></td>
</tr>
<tr>
<td>◆ Attention</td>
<td>◆ Dilated</td>
<td>◆ Layer</td>
<td></td>
</tr>
<tr>
<td>◆ Bilinear</td>
<td>◆ Transposed</td>
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<tr>
<td>◆ Sparse</td>
<td></td>
<td></td>
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<tr>
<td>◆ SDDMM</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>◆ SPMM</td>
<td></td>
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</tr>
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- **Pooling**
  - ◆ Max/Min/Avg
  - ◆ Adaptive

- **Loss**
  - ◆ NLL
  - ◆ BCE

- **Recurrent**
  - ◆ LSTM
  - ◆ GRU

- **TensorFlow**: > 400 operators
- **PyTorch**: > 200 operators
Various Data Types

Common tensor data types

- Float64
- Float32
- Float32
- Float32
- Float16
- BFloat16
- Int64
- Int32
- Int32
- Int16
- Int8
- Bool

For performance critical kernels:
#Implementations ≈ #Data types × #Kernels
Handwritten Code

➔ Low flexibility

◆ Fine-tune for every shape/data type/algorithm
◆ Employ assembly instructions
◆ ...

➔ High performance

◆ Apply sophisticated instruction/operator scheduling
◆ Simplify code
◆ ...


Handwritten Code is a Pain

→ For the company

◆ Hard to recruit new Machine Learning Engineers
◆ Difficult to maintain libraries

→ For the researchers

◆ A black box
  ● They want to understand how kernels work
  ● They want to fast validate new ideas at scale
Python-like Code

➔ **High** flexibility
   ✦ Build upon existing operators
   ✦ No need to recompile
   ✦ ...  

➔ **Low** performance
   ✦ Not fine-tuned for specific shapes
   ✦ Intermediate memory movement
   ✦ ...  

Can we design a language to achieve both high performance and flexibility?
Triton
A Programming Model for the Next Generation Deep Learning Systems
Programming Models for DNNs

Model
- PyTorch
- TensorFlow
- JAX

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Programming Models for DNNs

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- Triton
Inefficiencies of Existing PyTorch V1 Operators

➔ Individual kernels
  ◆ Can be slow
  ◆ Can run out-of-memory

➔ Graph compiler
  ◆ Don’t support custom data-structures
    • lists/trees of tensors
    • block-sparse tensors
  ◆ Don’t support custom precision format
  ◆ Automatic kernel fusion is limited

Solution: Employ Triton -> PyTorch V2
Triton is Designed to Achieve Both High Flexibility and Performance

➔ Flexibility

◆ A small core set of operations (~40 interface functions and ~20 core functions)
◆ Can be composed into almost all existing PyTorch operators (TorchInductor)
◆ SPMD but not SIMT

➔ Performance

◆ JIT generated kernels
◆ Handwritten PTX code
◆ Many passes to combine, simplify, and schedule operations
Triton Design

➔ PyTorch compatible
  ◆ Tensors are stored on-chip rather than off-chip
  ◆ Custom data-structures using tensors of pointers

➔ Python syntax
  ◆ All standard python control flow structure (for/if/while) are supported
  ◆ Python code is lowered to Triton IR
Write GPU Kernels Using Triton
GPU-accelerated Application Overview

➔ CPU and GPU execute asynchronously

➔ CPU dispatches commands to GPU
Terminologies

➔ Parallelism
  ◆ Grid
    ● One for each kernel
  ◆ Block/Warp/Thread

➔ Memory
  ◆ Global
    ● Visible to all threads
  ◆ Shared
    ● Private to each block
  ◆ Local
    ● Private to each thread
## CUDA vs Triton

<table>
<thead>
<tr>
<th>Feature</th>
<th>CUDA</th>
<th>Triton</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>Global/Shared/Local</td>
<td>Automatic</td>
</tr>
<tr>
<td>Parallelism</td>
<td>Threads/Blocks/Warps</td>
<td>Mostly Blocks</td>
</tr>
<tr>
<td>Tensor Core</td>
<td>Manual</td>
<td>Automatic</td>
</tr>
<tr>
<td>Vectorization</td>
<td>.8/.16/.32/.64/.128</td>
<td>Automatic</td>
</tr>
<tr>
<td>Async SIMT</td>
<td>Support</td>
<td>Limited</td>
</tr>
<tr>
<td>Device Function</td>
<td>Support</td>
<td>Not Available</td>
</tr>
</tbody>
</table>

Using Triton, you only need to know that a program is divided into multiple blocks.
Vector Addition (Single Block)

\[ Z[:] = X[:] + Y[:] \]

- Without boundary check

```python
import torch
import triton

@triton.jit
def _add(z_ptr, x_ptr, y_ptr, N):
    # same as torch.arange
    offsets = triton.arange(0, 1024)
    # create 1024 pointers to X, Y, Z
    x_ptrs = x_ptr + offsets
    y_ptrs = y_ptr + offsets
    z_ptrs = z_ptr + offsets
    # load 1024 elements of X, Y, Z
    x = triton.load(x_ptrs)
    y = triton.load(y_ptrs)
    # do computations
    z = x + y
    # write-back 1024 elements of X, Y, Z
    triton.store(z_ptrs, z)

N = 1024
x = torch.randn(N, device='cuda')
y = torch.randn(N, device='cuda')
z = torch.randn(N, device='cuda')
```

**Vector Addition (Single Block)**

- \[ Z[:] = X[:] + Y[:] \]
- Without boundary check
- **Kernel decorator**
- \[ \text{tl.load} \text{ and } \text{tl.store} \]
- Load/store values from global to shared/registers
- \[ _\text{add}[\text{grid}] (\text{num\_warps}=K) \]
- \[ \text{grid} = (G,) \]
- **G thread blocks**
- **num\_warps = K**
- K = 4 by default
Vector Addition (Boundary Check)

→ Z[:] = X[:] + Y[:]
  ◆ With boundary check
→ program_id()
  ◆ Get the block id
→ mask
  ◆ if mask[idx] is false, do not load
    the data at address pointer[idx]
→ triton.cdiv(N, 1024)
  ◆ (N – 1)/1024 + 1

@triton.jit
def _add(z_ptr, x_ptr, y_ptr, N):
  # same as torch.arange
  offsets = tl.arange(0, 1024)
  offsets += tl.program_id(0) * 1024
  # create 1024 pointers to X, Y, Z
  x_ptrs = x_ptr + offsets
  y_ptrs = y_ptr + offsets
  z_ptrs = z_ptr + offsets
  # load 1024 elements of X, Y, Z
  x = tl.load(x_ptrs, mask=offset<N)
  y = tl.load(y_ptrs, mask=offset<N)
  # do computations
  z = x + y
  # write-back 1024 elements of X, Y, Z

N = 192311
x = torch.randn(N, device='cuda')
y = torch.randn(N, device='cuda')
z = torch.randn(N, device='cuda')
grid = (triton.cdiv(N, 1024), )
_add[grid](z, x, y, N)
Vector Addition (Custom Tile Size)

→ Z[:] = X[:] + Y[:]
  ◆ Each block computes TILE elements
→ @triton.autotune
  ◆ Select the best config based on the execution time
  ◆ We don’t want to build complex autotune policies into Triton

@triton.jit
def _add(z_ptr, x_ptr, y_ptr, N):
    # same as torch.arange
    offsets = tl.arange(0, TILE)
    offsets += tl.program_id(0)*TILE
    # create 1024 pointers to X, Y, Z
    x_ptrs = x_ptr + offsets
    y_ptrs = y_ptr + offsets
    z_ptrs = z_ptr + offsets
    # load 1024 elements of X, Y, Z
    x = tl.load(x_ptrs, mask=offset<N)
    y = tl.load(y_ptrs, mask=offset<N)
    # do computations
    z = x + y
    # write-back 1024 elements of X, Y, Z
    tl.store(z_ptrs, z, mask=offset<N)

N = 192311
x = torch.randn(N, device='cuda')
y = torch.randn(N, device='cuda')
z = torch.randn(N, device='cuda')
Optimizing GPU Kernels
NVIDIA GA100 Architecture & Programming Challenges

➔ Multiple compute units
➔ Multiple memory spaces
➔ Multiple data types
➔ Thread synchronization/divergence
➔ Tensor cores
Techniques for Optimizing a GEMM Kernel

- **Vanilla (1-10% fp32 peak)**
  - +global memory coalesce
  - +shared memory

- **NVIDIA CUDA Programming Guide (30%-50% fp32 peak)**
  - +global memory coalesce
  - +shared memory

- **CUTLASS (80%-90% tf32 peak)**
  - +vectorization
  - +shared bank conflict reduction
  - +thread layout autotune
  - +async shared memory transfer
  - +multi-stage shared memory
  - +tf32 tensor core

- **cuBLAS (~90% tf32 peak)**
  - +register bank conflict reduction
  - +control code optimization

Difficulty:
- C++ Template & PTX
- C++/C
- SASS
Utilizing Tensor Cores - Layout

→ For each warp, we must load values into tiles of a specific layout to perform matrix multiplications

◆ Each data type could have multiple layouts
◆ Different data types (e.g., fp16 vs fp64) have different layouts

16x8x16 (fp16) 16x8x8 (fp16) 8x8x4 (fp64)
Swizzling tiles (T) when loading from global memory to avoid bank conflicts

Simple padding do not work because we need to read multiple tiles on different rows

**Utilizing Tensor Cores - Memory Swizzling**

---

<table>
<thead>
<tr>
<th>Phase 0</th>
<th>Phase 1</th>
<th>Phase 2</th>
</tr>
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<tbody>
<tr>
<td>T0</td>
<td>T0</td>
<td>T0</td>
</tr>
<tr>
<td>T1</td>
<td>T1</td>
<td>T1</td>
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<tr>
<td>T2</td>
<td>T2</td>
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<tr>
<td>T3</td>
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<tr>
<td>T4</td>
<td>T4</td>
<td>T4</td>
</tr>
<tr>
<td>T5</td>
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<tr>
<td>T0</td>
<td>T1</td>
<td>Tn-1</td>
</tr>
<tr>
<td>T1</td>
<td>T0</td>
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<td>T2</td>
<td>T3</td>
<td>T0</td>
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<tr>
<td>T3</td>
<td>T2</td>
<td>T5</td>
</tr>
<tr>
<td>T4</td>
<td>T5</td>
<td>T2</td>
</tr>
<tr>
<td>T5</td>
<td>T4</td>
<td>T7</td>
</tr>
</tbody>
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Utilizing Tensor Cores - ldmatrix & stmatrix

➔ Each thread provides a pointer to 128b row of data in Shared Memory
➔ A row is broadcast to four threads to match the arrangement of tensor cores

<table>
<thead>
<tr>
<th>Col0</th>
<th>col1</th>
<th>col2</th>
<th>col3</th>
<th>col4</th>
<th>col5</th>
<th>Col6</th>
<th>col7</th>
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</thead>
<tbody>
<tr>
<td>row0 %laneid = 0</td>
<td>%laneid = 1</td>
<td>%laneid = 2</td>
<td>%laneid = 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>dst=d0</td>
<td>dst=d0</td>
<td>dst=d0</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>row1 %laneid = 4</td>
<td>%laneid = 5</td>
<td>%laneid = 6</td>
<td>%laneid = 7</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>dst=d0</td>
<td>dst=d0</td>
<td>dst=d0</td>
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<td></td>
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<tr>
<td>row2 %laneid = 8</td>
<td>%laneid = 9</td>
<td>%laneid = 10</td>
<td>%laneid = 11</td>
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<tr>
<td></td>
<td>dst=d0</td>
<td>dst=d0</td>
<td>dst=d0</td>
<td></td>
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</tr>
<tr>
<td>row3 %laneid = 12</td>
<td>%laneid = 13</td>
<td>%laneid = 14</td>
<td>%laneid = 15</td>
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<td></td>
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</tr>
<tr>
<td>row4 %laneid = 16</td>
<td>%laneid = 17</td>
<td>%laneid = 18</td>
<td>%laneid = 19</td>
<td></td>
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<td>dst=d0</td>
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<td>dst=d0</td>
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<tr>
<td>row5 %laneid = 20</td>
<td>%laneid = 21</td>
<td>%laneid = 22</td>
<td>%laneid = 23</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td>dst=d0</td>
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<tr>
<td>row6 %laneid = 24</td>
<td>%laneid = 25</td>
<td>%laneid = 26</td>
<td>%laneid = 27</td>
<td></td>
<td></td>
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<td>dst=d0</td>
<td>dst=d0</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>row7 %laneid = 28</td>
<td>%laneid = 29</td>
<td>%laneid = 30</td>
<td>%laneid = 31</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>dst=d0</td>
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**Difficulty**

- Triton applies optimizations with minimal annotations required
- *C++ Template & PTX*
- *SASS*
Element-wise Operators

→ Triton and Torch both achieve peak bandwidth

→ Researchers can write *fused element-wise operators* easily using Triton
Fused Softmax

➔ Triton kernels can keep data on-chip throughout the entire softmax.

➔ PyTorch JIT could in theory do that but in practice doesn’t.

➔ The native PyTorch op is designed to work for every input shape and is slower in cases where we care.
Matrix Multiplication

→ It takes <25 lines of code to write a Triton kernel on par with cuBLAS

→ Arbitrary ops can be “fused” before/after the GEMM while the data is still on-chip, leading to large speedups over PyTorch
Fused Attention (Flash Attention)

➔ **From the author:** Triton is easier to understand and experiment with than CUDA

➔ Triton forward + backward is slightly slower than CUDA forward + backward
Kernl

➔ Run PyTorch transformer models several times faster on GPU with a single line of code
➔ The first OSS inference engine written in Triton
New Challenges With Hopper

- Tensor Memory Accelerator (TMA)
  - Transfer large blocks of data between global memory and shared memory

- Distributed Shared Memory
  - Direct communication between shared memory on different SMs

- Thread Block Cluster
  - Cluster -> Grid -> Block -> Warp

- FP8 Data Types and Mode (Transformer Engine)
  - Native FP8 tensor core
Triton-MLIR (Triton V2)
Goals

➔ Make Triton more robust
➔ Using existing infrastructure to avoid creating new wheels
➔ Support more backends
Features

→ MLIR (Multi-level intermediate representation)
  ◆ Triton dialect
  ◆ TritonGPU dialect

→ Clean layout concepts
  ◆ Distributed, Sliced, Blocked, Shared, DotOperand
  ◆ Adopted by CUTLASS (CuTe)

→ Low overhead runtime
  ◆ Cache and fetch kernels using efficient signatures

→ Debugging
  ◆ triton.language.print

→ Profiler interface
  ◆ Kernel launch hooks
  ◆ Compilation hooks
Multiple Frontends and Backends (In Progress)
Contributors

*Anthropic*
Da Yan

*Meta*
Shintaro Iwasaki

*Microsoft*
Ian Bearman

*NVIDIA*
Dongdong Li, Qingyi Liu, Chunwei Yan, Jun Yang, Chenggang Zhao, Ben Zhang, Goostavz Zhu
Takeaways

➔ Triton is designed to achieve both high performance and flexibility

➔ Triton V2 will be more robust than Triton V1

➔ Triton will support more backends other than NVIDIA GPUs soon
Thank You

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